CLAIMS

What is claimed is:

1. A system for testing a plurality of cores in an integrated circuit comprising:

a plurality of slave controllers, each of the plurality of slave controllers for testing at least one of the plurality of cores; and

a master controller coupled with the plurality of slave controllers in a star configuration, the master controller configured to allow test data to be input directly to a portion of the plurality of slave controllers in parallel, the portion of the plurality of slave controllers including more than one slave controller.

2. The system of claim 1 further comprising:

at least one AND gate coupled between the master controller and the plurality of slave controllers; and

wherein the master controller allows the test data to be input directly to the portion of the plurality of slave controllers by activating a portion of the at least one AND gate for the portion of the plurality of slave controllers.

3. The system of claim 2 further comprising:

at least one test data input coupled to the at least one AND gate.

4. The system of claim 2 wherein the master controller enables the portion of the at least one AND gate by providing an encoded address to an instruction register, the encoded address indicating the portion of the plurality of slave controllers.

5. The system of claim 4 wherein the encoded address includes a broadcast bit and a mask, the mask indicating the portion of the plurality of slave controllers.

6. The system of claim 5 wherein the master controller is further configured to enable a single slave controller.

7. The system of claim 1 wherein the master controller is a master TAP controller and wherein the plurality of slave controllers further includes a plurality of slave TAP controllers.

8. A system for testing a plurality of cores in an integrated circuit comprising:

a plurality of slave controllers, each of the plurality of slave controllers for testing at least one of the plurality of cores;

a master controller coupled with the plurality of slave controllers in a star configuration, the master controller configured to allow test data to be input directly to a portion of the plurality of slave controllers in parallel, the portion of the plurality of slave controllers including more than one slave controller;

a plurality of AND gates coupled between the plurality of slave controllers and the master controller; and

at least one test data input coupled with the plurality of AND gates, the master controller configured to provide an encoded address to enable a portion of the plurality of AND gates to couple a portion of the plurality of slave controllers to the at least one test data input in parallel, thereby allowing the test data to be input directly to the portion of the

plurality of slave controllers in parallel, the portion of the plurality of slave controllers including more than one slave controller.

9. A method for testing a plurality of cores in an integrated circuit, the plurality of cores being coupled with a plurality of slave controllers, the plurality of controllers coupled with a master controller in a star configuration, the plurality of slave controllers and the master controller being used in testing the plurality of cores, the method comprising:

(a) enabling a portion of the plurality of slave controllers to be able to directly receive test data in parallel, the portion of the plurality of slave controllers including more than one slave controller;

(b) providing the test data directly to the portion of the plurality of slave controllers while all of the portion of the plurality of slave controllers is enabled.

10. The method of claim 9 wherein the enabling step (a) further includes the steps of:

(a1) providing an encoded address.

11. The method of claim 10 wherein the encoded address providing step (a1) further includes the steps of:

(a1i) providing a broadcast bit, the broadcast bit indicating whether the more than one of the plurality of slave controllers is to be enabled; and

(a1ii) if more than one slave controller is to be enabled, providing a mask indicating the portion of the plurality of slave controllers.

12. The method of claim 11 wherein the encoded address providing step (a1) further includes the step of:

(a1ii) if only one slave controller is to be enabled, providing an address for a particular slave controller.

13. The method of claim 9 wherein at least one AND gate is coupled between the master controller and the plurality of slave controllers, and wherein the enabling step (a) further includes the step of:

(a1) enabling a portion of the at least one AND gate for the portion of the plurality of slave controllers.

14. The method of claim 9 wherein the master controller includes a master TAP controller and wherein the plurality of slave controllers includes a plurality of slave TAP controllers.

15. The method of claim 9 wherein the data providing step (b) further includes the step of:

(b1) providing the test data to the portion of the plurality of slave controllers in parallel.

16. A method for providing system for testing a plurality of cores in an integrated circuit, the method comprising:

(a) providing a plurality of slave controllers, each of the plurality of slave controllers for testing at least one of the plurality of cores; and

(b) providing a master controller coupled with the plurality of slave controllers in a star configuration, the master controller configured to allow test data to be input directly to a portion of the plurality of slave controllers in parallel, the portion of the plurality of slave controllers including more than one slave controller.

17. The method of claim 16 further comprising:

(c) providing at least one AND gate coupled between the master controller and the plurality of slave controllers;

wherein the master controller allows the test data to be input directly to the portion of the plurality of slave controllers by activating a portion of the at least one AND gate for the portion of the plurality of slave controllers.

18. The method of claim 17 further comprising:

(d) providing at least one test data input coupled to the at least one AND gate.

19. The method of claim 17 wherein the master controller providing step (b) further includes the step of:

(b1) configuring the master controller to enables the portion of the at least one AND gate by providing an encoded address to an instruction register, the encoded address indicating the portion of the plurality of slave controllers.

20. The method of claim 19 wherein the encoded address includes a broadcast bit and a mask, the mask indicating the portion of the plurality of slave controllers.

21. The method of claim 20 wherein the master controller providing step (b) further includes the step of:

(b2) configuring the master controller to allow the master controller to enable a single slave controller.